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PATENT
P56350

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

CHUL-MIN KIM

Serial No.:	09/832,199	Examiner:	ONUAKU, CHRISTOPHER O
Filed:	11 April 2001	Art Unit:	2616

For: METHOD FOR DESIGNING DE-EMPHASIS CIRCUIT FOR VIDEO SIGNAL PROCESSING INTEGRATED CIRCUIT AND INTEGRATED CIRCUIT MADE BY THE SAME

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O.Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with 37 C.F.R. §1.56, and §§1.97 and 1.98 as amended, Applicant cites, describes, and provides copies of the following art references. Under 37 C.F.R. §1.98(a)(2) however, copies of U.S. patent reference(s) are not provided.

US PATENT REFERENCE:

- United States Patent No. 4,641,206 to Iwafune, entitled *VIDEO SIGNAL RECORDING AND REPRODUCING APPARATUS INCLUDING A NOISE REDUCTION CIRCUIT*, issued on 3 February 1987.
- United States Patent No. 5,164,862 to Kawamata, entitled *AUTOMATIC RECORDING MODE DETECTING APPARATUS FOR USE IN VIDEO TAPE REPRODUCER*, issued on 17 November 1992.

FOREIGN PATENT REFERENCE:

- European Patent Publication No. 0 595 629 to Yamamoto, entitled *TRIMMING*

CIRCUIT, published on 4 May 1994 (with English abstract).

- European Patent Publication No. 0 472 065 to Russell, *et al.*, entitled *USER-PROOF POST-ASSEMBLY OFFSET VOLTAGE TRIM*, published on 26 February 1992 (with English abstract).

OTHER DOCUMENTS:

- European Office action for European Patent Application No. 01 30 2923, issued on 12 April 2006.
- An article "A SINGLE CHIP Y/C SIGNAL PROCESSING IC FOR VHS VCRS" written by Kawano, *et al.*, published in IEEE Transactions on Consumer Electronics, Vol. 35, No. 4, pp 741-747 on November 1989 (with English abstract).

DISCUSSION

Iwafune US'206, according to the European Office action in applicant's European patent application Serial No. 01 30 2923, discloses that a video signal recording and reproducing apparatus comprises a circuit for recording an FM recording video signal onto a recording medium, a demodulator for reproducing and demodulating the recorded signal from the recording medium back into the original video signal, a noise reduction circuit for reducing a noise component in the reproduced video signal. The noise reduction circuit has a first delay circuit for delaying the reproduced video signal by one horizontal scanning period (1H), a first differential amplifier supplied with the reproduced video signal and with a 1H delayed reproduced video signal, a first limiter for amplitude-limiting an output of the first differential amplifier, and a subtracting circuit for performing a subtraction between the reproduced video signal and an output of the first limiter. The apparatus further comprises a second differential amplifier supplied with the recording video signal to one input thereof, a second delay circuit for delaying the recording video signal by 1H and for supply a 1H delayed recording video signal to another input of the second differential amplifier, a second limiter for amplitude-limiting an output video signal component of the second differential amplifier to a limiting level approximately in the same range as a limiting level of the first limiter,

and an adding and mixing circuit for adding and mixing an output video signal component of the second limiter to the recording video signal.

Kawamata US'862, discloses that a video signal recording mode detecting apparatus is provided to detect a plurality of recording modes in which frequencies of the carriers in FM video signals are different. By counting the number of pulses that result from wave-shaping the carrier of an FM video signal during a predetermined period, it is possible to detect the particular video signal recording mode being employed. By using a digital detecting mode circuit recording modes having different carriers can be positively detected by relative small-scale circuits suitable for fabrication as integrated circuits.

Yamamoto EP'649, discloses that a trimming circuit has a plurality of zener zap diodes (Z_{11},Z_{12},Z_{13}), a group of switching devices (Q_{14},Q_{15},Q_{16}) for selectively zapping the zener zap diodes (Z_{11},Z_{12},Z_{13}), and a decoder circuit (B_{11}) for controlling the ON/OFF states of the switching devices (Q_{14},Q_{15},Q_{16}).

Russell EP'065, discloses that a post-assembly trim of a monolithic IC is set forth wherein selected package pins can be employed to address the on-chip trim circuit. Then, after the trim is completed, the circuit is addressed to provide a disconnect of the coupling between the trim pins and the post assembly trim circuit of the IC, while leaving the pins fully usable for other purposes. This means that following the post-assembly trim the trim pins cannot accidentally be employed for further trimming and the packaged IC is user-proof. A circuit that employs zener zapping for both trimming and disconnect is detailed and the invention is clearly usable for plastic encapsulated devices. However, when cavity containing packages are involved it is shown that a combination of zener zapping and fuse blowing can be employed.

Kawano, discloses that this paper describes a single chip video signal processor for VHS VCRs/ the chip includes all of the luminance and chrominance signal processers with four internal filters. these filters are automatically adjusted by chroma-PLL (phase locked loop).

Pursuant to 37 CFR §1.97(d), the undersigned attorney hereby certifies that each item of information contained in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign patent application not more than three (3) months prior to the filing of the statement.

The citation of the foregoing references is not intended to constitute an assertion that other or more relevant art does not exist. Accordingly, the Examiner is requested to make a wide-ranging and thorough search of the relevant art.

No fee is incurred by this Statement.

Respectfully submitted,

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	APPLICANT CHUL-MIN KIM	
	FILING DATE 11 April 2001	GROUP 2616

U.S. PATENT DOCUMENTS

EXAMINER	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE
	4,641,206	02/87	*Iwafune*			
	5,164,862	11/92	*Kawamata*			

FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO
	EP 0 595 629	05/94	EUROPE			Abstract	
	EP 0 472 065	02/92	EUROPE			Abstract	

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

	European Office Action of the European Patent Application No. 01 30 2923, issued on 12 April 2006
	An article "A SINGLE CHIP Y/C SIGNAL PROCESSING IC FOR VHS VCRS" written by Kawano, *et al.*, published in IEEE Transactions on Consumer Electronics, Vol. 35, No. 4, pp 741-747 on Nov ember 1989

EXAMINER: *DATE CONSIDERED:*

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP §609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.